


**DIE CROSS REFERENCE**

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH101A RH101A	RH101A DICE RH101A DWF

**PAD FUNCTION**

1. BAL/COMP
2. -IN
3. +IN
4. V<sup>-</sup>
5. BAL
6. OUT
7. V<sup>+</sup>
8. COMP

Backside (substrate) is an alloyed gold layer. May be connected to V<sup>-</sup> or no connection.

**DICE ELECTRICAL TEST LIMITS**

$T_A = 25^\circ\text{C}$ .  $V_S = \pm 20\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	$T_A = 25^\circ\text{C}$		UNITS
			MIN	MAX	
<b>Pre-Irradiation (Note 1)</b>					
$V_{OS}$	Input Offset Voltage	$R_S \leq 50\text{k}$		2	mV
$I_{OS}$	Input Offset Current			10	nA
$I_B$	Input Bias Current	$V_{CM} = 0\text{V}$		75	nA
$A_{VOL}$	Large Signal Voltage Gain	$V_S = \pm 15\text{V}$ , $V_{OUT} = \pm 10\text{V}$ , $R_L \geq 2\text{k}$	50		V/mV
CMRR	Common Mode Rejection Ratio	$R_S \leq 50\text{k}$	80		dB
PSRR	Power Supply Rejection Ratio	$R_S \leq 50\text{k}$	80		dB
	Input Voltage Range	$V_S = \pm 20\text{V}$	$\pm 15$		V
$V_{OUT}$	Output Voltage Swing	$V_S = \pm 15\text{V}$ , $R_L \geq 10\text{k}$	$\pm 12$		V
		$V_S = \pm 15\text{V}$ , $R_L \geq 2\text{k}$	$\pm 10$		V
$I_S$	Supply Current	$V_S = \pm 20\text{V}$		3	mA

# DICE/DWF SPECIFICATION

## RH101A

### DICE ELECTRICAL TEST LIMITS

$T_A = 25^\circ\text{C}$ .  $V_S = \pm 20\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	10Krad(SI)		20Krad(SI)		50Krad(SI)		100Krad(SI)		200Krad(SI)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
<b>Post-Irradiation (Note 4)</b>													
$V_{OS}$	Input Offset Voltage	$R_S \leq 50\text{k}$	2		2		2		2		3		mV
$I_{OS}$	Input Offset Current		10		10		10		10		20		nA
$I_B$	Input Bias Current		75		75		100		200		400		nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 15\text{V}$ , $R_S \leq 50\text{k}$	80		80		80		80		80		dB
PSRR	Power Supply Rejection Ratio	$V_{CM} = \pm 5\text{V}$ to $\pm 20\text{V}$ , $R_S \leq 50\text{k}$	80		80		80		80		80		dB
$A_{VOL}$	Large Signal Voltage Gain	$R_L = \pm 2\text{k}$ , $V_O = \pm 10\text{V}$ , $V_S = \pm 15\text{V}$	50		50		50		50		25		V/mV
$V_{OUT}$	Maximum Output Voltage Swing	$V_S = \pm 15\text{V}$ , $R_L \geq 10\text{k}$ $V_S = \pm 15\text{V}$ , $R_L \geq 2\text{k}$	$\pm 12$ $\pm 10$		$\pm 12$ $\pm 10$		$\pm 12$ $\pm 10$		$\pm 12$ $\pm 10$		$\pm 12$ $\pm 10$		V V
$I_S$	Supply Current	$V_S = \pm 20\text{V}$	3		3		3		3		3		mA

**Note 1:** Unless otherwise noted, all measurements are made with unity gain compensation ( $C_1 = 30\text{pF}$ ); these specifications apply for  $\pm 5\text{V} \leq V_S \leq 20\text{V}$ .

**Note 2:** For supply voltages less than  $\pm 15\text{V}$ , the maximum input voltage is equal to the supply voltage.

**Note 3:** Refer to LTC standard product data sheet for all other applicable information.

**Note 4:** The post-irradiation table is for lot qualification based on sample lot assembly and testing only. Contact LTC marketing for more detail.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-0101

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Linear Technology Corporation  
1630 McCarthy Blvd., Milpitas, CA 95035-7417  
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

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