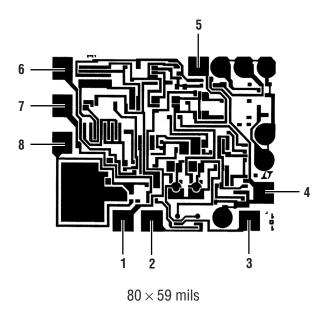
# DICE/DWF SPECIFICATION

# RH101A Operational Amplifier



Backside (substrate) is an alloyed gold layer. May be connected to  $V^-\,\mbox{or}$  no connection.

### **DIE CROSS REFERENCE**

LTC Finished	Order DICE CANDIDATE					
Part Number	Part Number Below					
RH101A	RH101A DICE					
RH101A	RH101A DWF					

#### PAD FUNCTION

- 1. BAL/COMP
- 2. -IN
- 3. +IN
- 4. V<sup>-</sup>
- 5. BAL
- 6. OUT
- 7. V+
- 8. COMP

## **DICE ELECTRICAL TEST LIMITS**

## $T_A$ = 25°C. $V_S$ = $\pm 20 V$ unless otherwise noted.

			T <sub>A</sub> = 25°C	
SYMBOL	PARAMETER	CONDITIONS	MIN MAX	( UNITS
Pre-Irradiation	ı (Note 1)			
V <sub>OS</sub>	Input Offset Voltage	R <sub>S</sub> ≤ 50k	2	mV
I <sub>0S</sub>	Input Offset Current		10	nA
I <sub>B</sub>	Input Bias Current	V <sub>CM</sub> = 0V	75	nA
A <sub>VOL</sub>	Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V, R_L \ge 2k$	50	V/mV
CMRR	Common Mode Rejection Ratio	$R_S \le 50k$	80	dB
PSRR	Power Supply Rejection Ratio	$R_S \le 50k$	80	dB
	Input Voltage Range	V <sub>S</sub> = ±20V	±15	V
V <sub>OUT</sub>	Output Voltage Swing	$V_S = \pm 15V, R_L \ge 10k$	±12	V
		$V_S = \pm 15V, R_L \ge 2k$	±10	V
Is	Supply Current	$V_S = \pm 20V$	3	mA

# DICE/DWF SPECIFICATION

## RH101A

## **DICE ELECTRICAL TEST LIMITS**

 $T_A = 25^{\circ}C$ .  $V_S = \pm 20V$  unless otherwise noted.

			10Kra	10Krad(SI)		20Krad(SI)		50Krad(SI)		100Krad(SI)		200Krad(SI)	
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Post-Irrad	iation (Note 4)		·										
V <sub>OS</sub>	Input Offset Voltage	$R_S \le 50k$		2		2		2		2		3	mV
I <sub>OS</sub>	Input Offset Current			10		10		10		10		20	nA
I <sub>B</sub>	Input Bias Current			75		75		100		200		400	nA
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 15V, R_S \le 50k$	80		80		80		80		80		dB
PSRR	Power Supply Rejection Ratio	$V_{CM} = \pm 5V \text{ to } \pm 20V,$ $R_S \le 50k$	80		80		80		80		80		dB
A <sub>VOL</sub>	Large Signal Voltage Gain	$R_L = \pm 2k, V_0 = \pm 10V,$ $V_S = \pm 15V$	50		50		50		50		25		V/mV
V <sub>OUT</sub>	Maximumm Output Voltage Swing	$V_S = \pm 15V, R_L \ge 10k$ $V_S = \pm 15V, R_L \ge 2k$	±12 ±10		±12 ±10		±12 ±10		±12 ±10		±12 ±10		V
Is	Supply Current	V <sub>S</sub> = ±20V	3		3		3		3		3		mA

**Note 1:** Unless otherwise noted, all measurements are made with unity gain compensation (C1 = 30pF); these specifications apply for  $\pm 5V \le V_S \le 20V$ 

**Note 2:** For supply voltages less than  $\pm 15V$ , the maximum input voltage is equal to the supply voltage.

**Note 3:** Refer to LTC standard product data sheet for all other applicable information.

**Note 4:** The post-irradiation table is for lot qualification based on sample lot assembly and testing only. Contact LTC marketing for more detail.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-0101